AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of the Claims:

Claims 1-8. (Canceled)

9. (New) A semiconductor wafer comprising:

chip areas, each of which at least has

(i) a memory matrix;

(ii) a first terminal;

(iii) a second terminal; and

(iv) a further terminal,

wherein the first terminal is coupled to receive a signal for judging electric connection/non-connection between a needle connected to a test apparatus at burn-in and the further terminal provided in each of the chip areas, and

wherein the second terminal is for outputting a response signal in accordance with the signal applied to the first terminal.

10. (New) The semiconductor wafer according to claim 9,

wherein the memory matrix corresponds to a volatile memory.

11. (New) The semiconductor wafer according to claim 9,

wherein the memory matrix corresponds to a nonvolatile memory.

12. (New) The semiconductor wafer according to claim 9,

wherein the further terminal is a test input/output (I/O) external chip terminal.

13. (New) A semiconductor wafer comprising:

chip areas, each of which at least has

(i) a memory matrix including memory cells;

(ii) address input terminals coupled to receive an address signal specifying an address of one of the memory cells in the memory matrix;

(iii) data input/output terminals for inputting and outputting write data and read data to and from the memory matrix;

(iv) control signal terminals coupled to receive control signals for controlling write and read operations of the memory matrix; and

(v) test-only signal terminals for inputting signals for judging electric connection/non-connection between a needle connected to a test apparatus at burn-in and a terminal provided in each of the chip areas.

14. (New) The semiconductor wafer according to claim 13,

wherein the memory cells are volatile memory cells.

15. (New) The semiconductor wafer according to claim 13,

wherein the memory cells are nonvolatile memory cells.

16. (New) A semiconductor chip comprising:

a memory circuit including a memory matrix;

a terminal; and

a test circuit for receiving a signal for judging electric connection/non-connection between a needle connected to a test apparatus at burn-in and the terminal of the semiconductor chip, and providing a response signal for responding to the signal received by the test circuit, and based on the response signal judging electric connection/non-connection between the needle connected to the test apparatus at the burn-in and the terminal of the semiconductor chip.

17. (New) The semiconductor chip according to claim 16,

wherein said test circuit comprises:

a test clock terminal to be inputted with a test clock signal;

first and second test control terminals to be inputted with a test control signal, respectively;

a test terminal to and from which test input/output data is to be inputted and outputted;

a first power terminal to be supplied with a first power supply voltage; and

a second power terminal to be supplied with a second power supply voltage.

18. (New) The semiconductor chip according to claim 17,

wherein the memory matrix corresponds to a volatile memory or a nonvolatile memory.

19. (New) The semiconductor chip according to claim 17,

wherein the test circuit is adapted to synchronize the test clock signal inputted from the test clock terminal in accordance with test control signals inputted from the first and second test control terminals, and includes a shift register for shifting test command data being input from the test input/output terminal and a decoder for decoding data of the shift register, wherein operation of a test mode is initiated in accordance with a current status flag and a concurrent status flag being outputted from the decoder.

20. (New) The semiconductor chip according to claim 19,

wherein the test circuit further includes a counter for counting synchronously the test clock signal being input from the test dock terminal, and uses a count value of the counter as an address signal of the memory circuit at said test mode, and outputs a carry signal of the counter from the test input/output terminal to thereby judge electric connection/non-connection between each needle and each terminal of the semiconductor chip in the test apparatus.

21. (New) The semiconductor chip according to claim 20,

wherein the carry signal of the counter is used as write data of the memory circuit.

22. (New) The semiconductor chip according to claim 20,

wherein the carry signal of the counter and the read data of the memory circuit are operated on by an exclusive logic circuit, the result of which is output from the test input/output terminal, which is used to monitor bad chip rate during said burn-in.

23. (New) A method of manufacturing a semiconductor device, comprising:

producing a first semiconductor wafer including first semiconductor chips;

producing a second semiconductor wafer including second semiconductor chips;

performing burn-in of the first and the second semiconductor wafer;

cutting the first and second semiconductor wafers to produce a batch of first semiconductor chips and a batch of second semiconductor chips, respectively; and

assembling one of the first semiconductor chips and one of the second semiconductor chips to produce the semiconductor device.

24. (New) The method of manufacturing a semiconductor device according to claim 23,

wherein performance of the burn-in comprises:

performing a contact check for judging electric connection/non-connection between each needle connected to a test apparatus and each

terminal provided in each of the first and second semiconductor chips of the first and second semiconductor wafers.

25. (New) The method of manufacturing a semiconductor device according to claim 23,

wherein assembling includes a process of forming a stacked arrangement of one or more of the first semiconductor chips and one or more of the second semiconductor chips on a substrate to produce the semiconductor device and providing prescribed electrical connections therebetween.

26. (New) The method of manufacturing a semiconductor device according to claim 25,

wherein the substrate is a wiring substrate.

27. (New) The method of manufacturing a semiconductor device according to claim 23,

wherein each of the first semiconductor chips includes a volatile memory and each of the second chips includes a nonvolatile memory.